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EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
2633	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,227	TAGA ET AL.	
	Examiner	Art Unit	
	David S. Kim	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20,22-25 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-34* is/are allowed.

6)☒ Claim(s) *20,22-25 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant's compliance with the objections to the specification in the previous Office Action (mailed on 27 July 2005) is noted and appreciated. Applicant responded by amending the cross reference in the specification and by amending the abstract. Applicant's response obviates the previous objections. The previous objections are withdrawn.

Claim Objections

2. Applicant's compliance with the objection to claim 25 in the previous Office Action (mailed on 27 July 2005) is noted and appreciated. Applicant responded by amending claim 25. Applicant's response obviates the previous objection, and the previous objection is withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Kiyonaga et al.

4. **Claims 20, 22-23, and 25** are rejected under 35 U.S.C. 102(b) as being anticipated by Kiyonaga et al. (U.S. Patent No. 5,652,767, hereinafter "Kiyonaga").

Regarding claim 20, Kiyonaga discloses:

An optical receiving apparatus, comprising:

a photodetector (photo-diode 22_{n+1} in Fig. 16) for converting an optical signal input from an optical transmission line to an electrical signal;

a clock extractor (notice clock output from preamplifier 23_{n+1}, col. 15, l. 35-38) for extracting a clock from the electrical signal;

a threshold controller (circuit 88) programmed with information about clock amplitude versus threshold characteristics and for collating an amplitude of the extracted clock with the clock amplitude versus threshold characteristics (the average of the clock amplitude corresponds to the threshold voltage to limiter amplifier 24_{n+1}, col. 15, l. 36-41, e.g., as the amplitude of the extracted clock increases, the average increases and, thus, the threshold voltage increases) and for determining and providing to the discriminator a discrimination threshold; and

a discriminator (limiter amplifier 24_{n+1}) for discriminating the electrical signal by applying to the electrical signal the determined discrimination threshold.

Regarding claim 22, Kiyonaga discloses:

The optical receiving apparatus of claim 20, further comprising a signal brancher (circuit node after preamplifier 23_{n+1} in Fig. 16) for branching the electrical signal from the photodetector to a first electrical signal component (circuit 88) and a second electrical signal component (limiter amplifier 24_{n+1}).

Regarding claim 23, Kiyonaga discloses:

The optical receiving apparatus of claim 22, wherein the signal brancher simultaneously (no delay is indicated in the circuit in Fig. 16) applies the electrical signal from the photodetector to the discriminator and the clock extractor.

Regarding claim 25, Kiyonaga discloses:

A method for optical reception, comprising:

converting optical signal input from an optical transmission line to an electrical signal (photo-diode 22_{n+1} in Fig. 16);

extracting a clock from the electrical signal (notice clock output from preamplifier 23_{n+1}, col. 15, l. 35-38);

storing information about clock amplitude versus threshold characteristics (circuit 88 is designed to correspond the average of the clock amplitude to the threshold voltage to limiter amplifier 24_{n+1}, col. 15, l. 36-41);

determining a discrimination threshold by collating an amplitude of the extracted clock with the stored information about clock amplitude versus threshold characteristics (the average of the clock amplitude corresponds to the threshold voltage to limiter amplifier 24_{n+1}, col. 15, l. 36-41, e.g., as the amplitude of the extracted clock increases, the average increases and, thus, the threshold voltage increases);

providing the determined discrimination threshold to a discriminator (provision of the threshold voltage to limiter amplifier 24_{n+1}, col. 15, l. 36-41);

discriminating the electrical signal by applying the determined discrimination threshold to the electrical signal (limiter amplifier 24_{n+1}).

Regarding claim 27, Kiyonaga discloses:

The optical receiving apparatus of claim 20, wherein the threshold controller determines the discrimination threshold by moving the discrimination threshold to a space side when the clock amplitude decreases (a lower clock amplitude decreases the average, which decreases the threshold voltage, thus moving the threshold to a space "0" side) and moving the discrimination threshold to a mark side when the clock amplitude increases (a higher clock amplitude increases the average, which increases the threshold voltage, thus moving the threshold to a mark "1" side).

Tomofuji et al.

5. **Claims 20 and 22** are rejected under 35 U.S.C. 102(e) as being anticipated by Tomofuji et al. (U.S. Patent No. 6,496,552 B2, hereinafter "Tomofuji").

Regarding claim 20, Tomofuji discloses:

An optical receiving apparatus, comprising:

a photodetector (optoelectric conversion circuit 1 in Fig. 19) for converting an optical signal input from an optical transmission line to an electrical signal;

a clock extractor (clock signal generator 34 in Fig. 15) for extracting a clock from the electrical signal;

a threshold controller (circuits 32-33 in Fig. 15) programmed with information about clock amplitude versus threshold characteristics and for collating an amplitude of the extracted clock with the clock amplitude versus threshold characteristics (Figs. 6A, 16-17, col. 16, l. 10 – col. 17, l. 46; maximum amplitude corresponds to 100% duty, which corresponds to reference level Vro in Fig. 6A; lower amplitude corresponds to lower than 100% duty or higher than 100% duty , which corresponds to reference level smaller than Vro or to reference level Vru in Fig. 6A, respectively) and for determining and providing to the discriminator a discrimination threshold (signal "ref" in Fig. 15); and

a discriminator (circuit 31 in Fig. 15) for discriminating the electrical signal by applying to the electrical signal the determined discrimination threshold.

Regarding claim 22, Tomofuji discloses:

The optical receiving apparatus of claim 20, further comprising a signal brancher (circuit node after equalizing amplifier 2 in Fig. 19) for branching the electrical signal from the photodetector to a first electrical signal component (timing circuit 3) and a second electrical signal component (discriminating circuit 4).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyonaga.

Regarding claim 24, Kiyonaga does not expressly disclose:

The optical receiving apparatus of claim 22, wherein the signal brancher selectively applies the electrical signal from the photodetector to the discriminator and the clock extractor.

However, selective application of signals is an extremely common practice in the art. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to arrange the signal brancher to selectively apply the electrical signal from the photodetector to the discriminator and the clock extractor. One of ordinary skill in the art would have been motivated to do this to choose when to receive signals or not. For example, if one would like to turn off the receiving device to save power or to cease communication, one would select to not apply the signal to components. Such selection could occur at any number of locations along the signal lines of Kiyonaga, including the signal brancher.

Allowable Subject Matter

9. **Claims 28-34** are allowed.

Response to Arguments

10. Applicant's arguments, filed on 31 October 2005 with regard to claims 20, 22-25, and 27 (p. 11-15), have been fully considered but they are not persuasive. Applicant presents arguments against Kiyonaga and Tomofuji.

Regarding a first point against Kiyonaga, Applicant states,

> "First, for the reasons provided above, Kiyonaga does not teach 'a threshold controller programmed with information about clock amplitude versus threshold characteristics and for collating an amplitude of the extracted clock with the clock amplitude versus threshold characteristics.' (Emphasis Added). Instead, Kiyonaga teaches detecting an average level of a clock, and not an 'amplitude' of the clock. (Col. 15, lines 36-38)" (p. 12, 1st full paragraph).

Regarding Applicant's point about "amplitude" and "average level" of a clock, in the environment of Kiyonaga, the "level" of the clock is synonymous with the "amplitude" of the clock. Accordingly, Kiyonaga employs the average "amplitude" of the clock. This average clock "amplitude" is correlated with the threshold voltage of Kiyonaga (col. 15, l. 36-41). Thus, Applicant's point about "amplitude" and "average level" of a clock is not persuasive.

Regarding a second point against Kiyonaga, Applicant states,

> "Second, neither Kiyonaga nor Tomofuji teach 'a threshold controller programmed with information about clock amplitude versus threshold characteristics and for collating an amplitude of the extracted clock with the clock amplitude versus threshold characteristics.' (Emphasis Added).
>
> Kiyonaga teaches an average detecting circuit 88 merely receiving an average level of the clock from the pre-amplifier 23n+1 and the average level of the clock being merely 'supplied, as a threshold voltage for the clock, to the limiter amplifier 24n+1. (Col. 15, lines 36-40). Accordingly, Kiyonaga teaches the average detecting circuit merely passing the average detected level to the limiter amplifier. The average detecting circuit does not collate the average detecting level with average detecting level versus threshold characteristics. Further, the average detecting circuit is not programmed with average detecting level versus threshold characteristics. Therefore, amended claim 20 is not anticipated by Kiyonaga" (p. 12, 2nd full paragraph – p. 13, 1st paragraph).

Regarding Applicant's point about the threshold controller being "programmed", note that the purpose of circuit 88 is to detect the average level of the clock from the simple input of the clock signal. Such a purpose implies that this circuit is *programmed* to calculate the average level of the clock from the simple input of the clock signal. Thus, Applicant's point about the threshold controller not being "programmed" is not persuasive.

Regarding Applicant's point about the threshold controller "collating", note that the controller expresses clock amplitude versus threshold characteristics through the average of the clock amplitude (col. 15, l. 36-41). That is, the controller maps higher clock amplitudes with higher threshold values since higher clock amplitudes lead to higher average values of the clock amplitude. Conversely, the controller maps lower clock amplitudes with lower threshold values since lower clock amplitudes lead to lower average values of the clock amplitude. Thus, Applicant's point about the threshold controller not "collating" is not persuasive.

> **Regarding a third point against Kiyonaga**, Applicant states,
>
> "Additionally, amended claim 25 includes, among other limitations, 'storing information about clock amplitude versus threshold characteristics.' (Emphasis Added). As noted above, the only stored table that the Applicants can find taught by Tomofuji correlates the average value of the data signal Vm, not the signal output from the synchronous detector, with the output reference level. (Col. 10, lines 25-40; FIG. 4).
>
> Accordingly, amended claim 25 is not anticipated by Kiyonaga nor Tomofuji and therefore amended claim 25 is patentable over these references" (p. 14, 3rd –4th paragraphs).

Regarding Applicant's point about "storing information", note that usage of the apparatus of Kiyonaga includes the step of "storing information" about clock amplitude versus threshold

characteristics. That is, the arrangement of average level detecting circuit 88 providing the threshold value constitutes this step of "storing information". More exactly, the apparatus "stores" the "information" that the average clock amplitude correlates to the threshold by arranging circuit 88 to use the average value that it detects as the threshold voltage to limiter amplifier 24_{n+1} (col. 15, l. 36-41). Thus, Applicant's point about not "storing information" is not persuasive.

Regarding a first point against Tomofuji, Applicant states,

> "[N]either Kiyonaga nor Tomofuji teach 'a threshold controller programmed with information about clock amplitude versus threshold characteristics and for collating an amplitude of the extracted clock with the clock amplitude versus threshold characteristics.' (Emphasis Added)." (p. 12, 2nd full paragraph).
>
> "Tomofuji teaches 'the reference signal generator 33b of the control circuit 33 generates a reference signal Vr by amplifying the signal output from the synchronous detector 32.' (Col. 17, lines 31-34). (Emphasis Added). Accordingly, Tomofuji teaches merely amplifying the signal output and eventually passing a version of the amplified signal to the amplifier 31a. Further, the control circuit table taught in Tomofuji correlates the average value of the data signal Vm, not the signal output from the synchronous detector, with the output reference level. (Col. 10, lines 25-40; FIG. 4). As similar to the case with Kiyonaga, the Applicants can find not teaching in Tomofuji of the reference generator collating the synchronous detector output with synchronous detector output versus threshold characteristics. Nor can the Applicants find teaching in Tomofuji of the reference generator being programmed with synchronous detector output versus threshold characteristics. Therefore, amended claim 20 is not anticipated by Tomofuji" (p. 13, 1st full paragraph).

Regarding Applicant's point about the threshold controller being "programmed", note that the purpose of circuits 32-33 in Fig. 15 of Tomofuji is to apply the following relationship between the clock amplitude and threshold characteristics: maximum amplitude corresponds to 100% duty, which corresponds to threshold/reference level Vro in Fig. 6A; lower amplitude corresponds to lower than 100% duty or higher than 100% duty, which corresponds to threshold/reference level smaller than Vro or to threshold/reference level Vru in Fig. 6A, respectively (Figs. 6A, 16-17, col. 16, l. 10 – col. 17, l. 46). Such a purpose implies that circuits 32-33 are *programmed* with information about clock amplitude versus threshold characteristics. The "amplifying" mentioned by Applicant is part of the *program* implemented by circuits 32-33 to control the threshold. Thus, Applicant's point about the threshold controller not being "programmed" is not persuasive.

Regarding Applicant's point about the threshold controller "collating", note again the relationship between the clock amplitude and threshold characteristics in Tomofuji: maximum amplitude corresponds

to 100% duty, which corresponds to threshold/reference level Vro in Fig. 6A; lower amplitude corresponds to lower than 100% duty or higher than 100% duty, which corresponds to threshold/reference level smaller than Vro or to threshold/reference level Vru in Fig. 6A, respectively (Figs. 6A, 16-17, col. 16, l. 10 – col. 17, l. 46). Circuits 32-33 "collate" the extracted clock amplitude with these "corresponding" relationships between the clock amplitude and threshold characteristics to control the threshold. The standing rejection under Tomofuji does not rely on the control circuit table of Tomofuji mentioned by Applicant. Thus, Applicant's point about the threshold controller not "collating" is not persuasive.

Regarding a second point against Tomofuji, Applicant states,

> "Additionally, amended claim 25 includes, among other limitations, 'storing information about clock amplitude versus threshold characteristics.' (Emphasis Added). As noted above, the only stored table that the Applicants can find taught by Tomofuji correlates the average value of the data signal Vm, not the signal output from the synchronous detector, with the output reference level. (Col. 10, lines 25-40; FIG. 4).
>
> Accordingly, amended claim 25 is not anticipated by Kiyonaga nor Tomofuji and therefore amended claim 25 is patentable over these references" (p. 14, 3rd –4th paragraphs).

Regarding Applicant's point about "storing information", note that claim 25 was not rejected under Tomofuji in the previous Office Action (mailed on 27 July 2005). Also, claim 25 is still not rejected under Tomofuji in the present Office Action. Thus, Applicant's point against Tomofuji and "storing information" is moot.

Summarily, Applicant's arguments against Kiyonaga and Tomofuji regarding claims 20, 22-25, and 27 are not persuasive. Thus, Examiner respectfully maintains the standing rejections.

Conclusion

11. The reference made of record and not relied upon is considered pertinent to applicant's disclosure. Han et al. is cited to show a receiver with a threshold controller that determines a discrimination threshold based on the intensity of the input optical signal (e.g., Fig. 4 and 8).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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